EE105 – Fall 2014
Microelectronic Devices and Circuits

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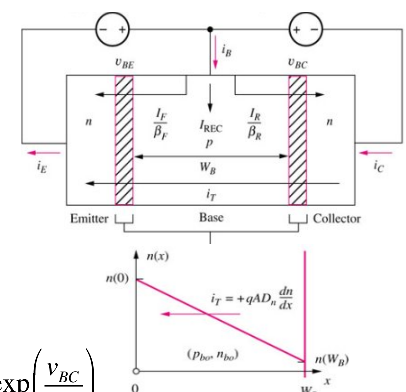
Minority Carrier Transport in the Base Region

- **BJT current dominated by diffusion of minority carriers (electrons in npn and holes in pnp transistors) across base region.**
- **Base current consists of hole injection back into emitter and collector and a small additional current to replenish holes lost to recombination with electrons in base.**
- **Minority carrier concentrations at the two ends of the base region are:**

$$n(0) = n_{bo} \exp\left(\frac{v_{BE}}{V_T}\right) \quad \text{and} \quad n(W_B) = n_{bo} \exp\left(\frac{v_{BC}}{V_T}\right)$$

n_{bo} is equilibrium electron density in the *p*-type base region.



Minority Carrier Transport in Base for npn

- **For narrow base devices, minority carrier density decreases linearly across the base, and the diffusion current in the base is:**

$$I_C \approx qAD_n \frac{dn}{dx} = qAD_n \frac{n(0)-n(W_B)}{W_B} = \frac{qAD_n}{W_B} n_{b0} \exp\left(\frac{v_{BE}}{V_T}\right)$$

$$\Rightarrow I_S = qAD_n \frac{n_{bo}}{W_B} = \frac{qAD_n}{W_B} \frac{n_i^2}{N_{AB}}$$

A : emitter area

D_n : electron diffusion coefficient

W_B : base width

$n_{b0} = \frac{n_i^2}{N_{AB}}$: equilibrium electron concentration in base (minority carrier)

N_{AB} : acceptor doping concentration in base

n_i : intrinsic carrier concentration (=10^{10} cm^{-3} for Si)

Mass-action law: $n \cdot p = n_i^2$ at equilibrium

Minority Carrier Transport in Base for pnp

- **Saturation current for the pnp transistor is**

$$I_S = qAD_p \frac{p_{bo}}{W_B} = \frac{qAD_p}{W_B} \frac{n_i^2}{N_{DB}}$$

A : emitter area

D_n : electron diffusion coefficient

W_B : base width

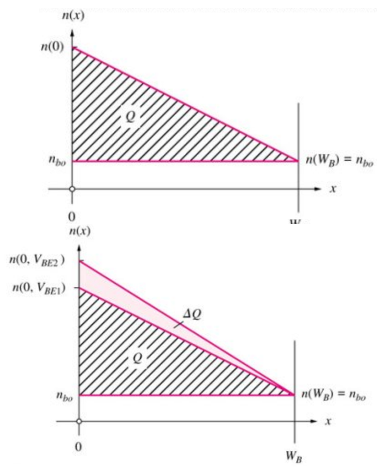
$p_{b0} = \frac{n_i^2}{N_{DB}}$: electron concentration in base (minority carrier)

N_{DB} : donor concentration in base

n_i : intrinsic carrier concentration (=10^{10} cm^{-3} for Si)

- **Due to higher mobility of electrons than holes, the npn transistor conducts higher current than the pnp for a given set of applied voltages.**

Base Transit Time



- **Forward transit time τ_F is the time constant associated with storing minority-carrier charge Q in base**

$$Q = qAn_{bo}\left[\exp\left(\frac{v_{BE}}{V_T}\right)-1\right]\frac{W_B}{2}$$

$$i_T = \frac{qAD_n}{W_B}n_{bo}\left[\exp\left(\frac{v_{BE}}{V_T}\right)-1\right]$$

$$\tau_F = \frac{Q}{i_T} = \frac{W_B^2}{2D_n} = \frac{W_B^2}{2\mu_n V_T}$$

Note: D_n and μ_n are related by

Einstein relation: $\dfrac{D_n}{\mu_n} = \dfrac{kT}{q} = V_T$

- **Transit time places upper limit on useful operating frequency of transistor.**

Diffusion Capacitance

- **For v_{BE} and hence i_C to change, charge stored in base region must also change.**
- **Diffusion capacitance in parallel with forward-biased base -emitter diode models the change in charge with v_{BE}.**

$$C_D = \left.\frac{dQ}{dv_{BE}}\right|_{Q-pt} = \frac{1}{V_T}\frac{qAn_{bo}W_B}{2}\exp\left(\frac{V_{BE}}{V_T}\right) = \frac{I_T}{V_T}\tau_F$$

- **Since transport current normally represents collector current in forward-active region,**

$$C_D = \frac{I_C}{V_T}\tau_F$$

Cutoff-Frequency, Transconductance and Transit Time

- **Forward-biased diffusion and reverse-biased pn junction capacitances of the BJT cause current gain to be frequency -dependent.**
- **Unity gain frequency f_T (or gain-bandwidth product):**

$$\beta(f) = \frac{\beta_F}{\sqrt{1+\left(\frac{f}{f_B}\right)^2}} \qquad \text{where} \quad f_B = \frac{f_T}{\beta_F} \quad \text{is the gain cutoff-frequency}$$

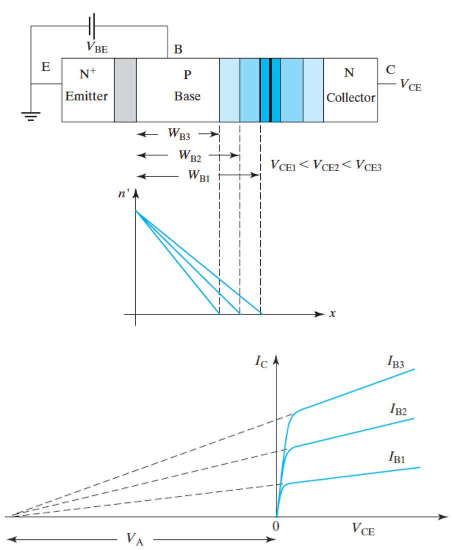
- **Transconductance is defined by:**

$$g_m = \left.\frac{di_C}{dv_{BE}}\right|_{Q-Pt} = \left.\frac{d}{dv_{BE}}\left[I_S \exp\left(\frac{v_{BE}}{V_T}\right)\right]\right|_{Q-Pt} = \frac{I_C}{V_T}$$

- **Transit time is given by:**

$$\tau_F = \frac{C_D}{g_m} \quad \Rightarrow \quad \omega_T = 2\pi f_T = \frac{1}{\tau_F} = \frac{g_m}{C_D}$$

Early Effect and Early Voltage



$$i_C = \frac{qAD_n}{W_B} n_{bo}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

As v_{CE} increases,

BC junction is more reverse-biased

$\Rightarrow$ BC junction depletion width increases

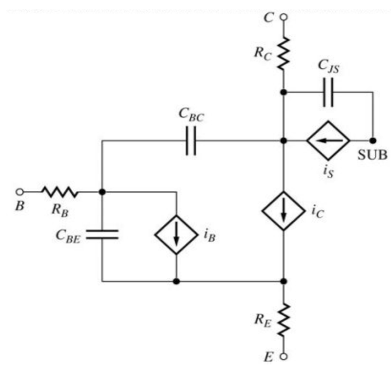
$\Rightarrow$ Base width decreases

$\Rightarrow$ i_C increases since $i_C \propto \frac{1}{W_B}$

This can be modeled by Early voltage:

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right)\left[1 + \frac{v_{CE}}{V_A}\right]$$

BJT SPICE Model

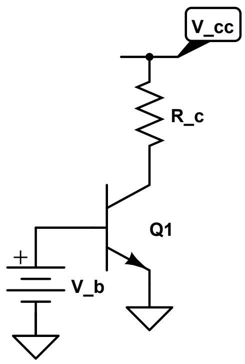


- Besides capacitances associated with the physical structure, additional components are:
  - diode current i_S and substrate capacitance C_{JS} related to the large area *pn* junction that isolates the collector from the substrate and one transistor from the next.
- R_B is resistance between external base contact and intrinsic base region.
- Collector current must pass through R_C on its way to the active region of the collector-base junction.
- R_E models any extrinsic emitter resistance in device.

Typical Values of BJT SPICE Model Parameters

- Saturation Current $I_S = 3\text{x}10^{-17}$ A
- Forward current gain $\beta_F = 100$
- Reverse current gain $\beta_R = 0.5$
- Forward Early voltage $V_{AF} = 75$ V
- Base resistance $R_B = 250\ \Omega$
- Collector Resistance $R_C = 50\ \Omega$
- Emitter Resistance $R_E = 1\ \Omega$
- Forward transit time $T_T = 0.15$ ns
- Reverse transit time $T_R = 15$ ns

BJT Bias: (1) Voltage Source to Base



$$I_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right)$$

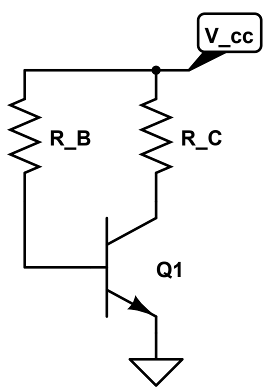
I_C varies exponentially with v_{BE} and V_T

Very sensitive to bias voltages and temperature

Also sensitive to I_S

Not desirable!

BJT Bias: (2) Bias with V_{CC} and Resistor



$$I_B = \frac{V_{CC} - v_{BE}}{R_B}$$

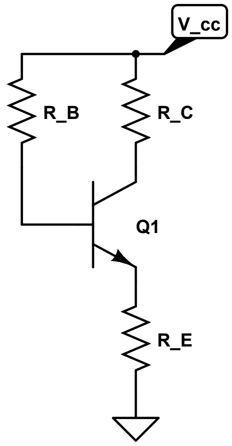
$$I_C = \beta I_B = \frac{V_{CC} - v_{BE}}{R_B/\beta}$$

Since $V_{CC} >> v_{BE}$, I_C is less sensitive to v_{BE}

It's also not sensitive to V_T or I_S

However, it is very sensitive to β

BJT Bias: (3) Bias with V_{CC} and R_B Plus R_E



KVL:

$$V_{CC} = I_B R_B + v_{BE} + I_E R_E$$

$$= \frac{I_C}{\beta} R_B + v_{BE} + \frac{I_C}{\alpha} R_E$$

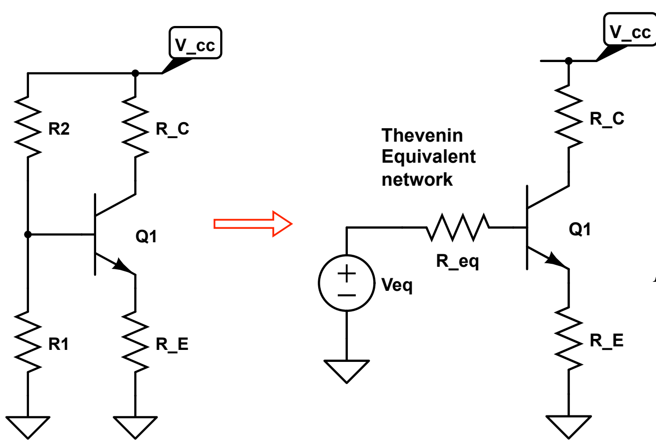
$$I_C = \frac{V_{CC} - v_{BE}}{\frac{R_B}{\beta} + \frac{R_E}{\alpha}}$$

Since $V_{CC} >> v_{BE}$, I_C is not sensitive to v_{BE}

$\frac{R_B}{\beta} << \frac{R_E}{\alpha}$, It's not sensitive to β

Both are good.

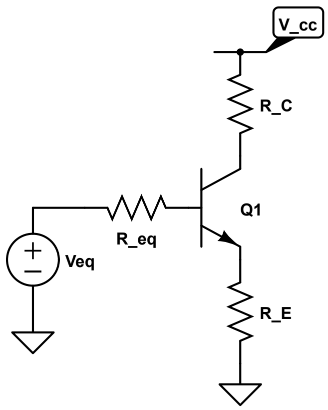
BJT Bias: (4) Four-Resistor Bias



$$V_{EQ} = V_{CC} \frac{R_1}{R_1 + R_2}$$

$$R_{EQ} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

BJT Bias: (4) Four-Resistor Bias



$$I_C = \frac{V_{EQ} - v_{BE}}{\frac{R_{EQ}}{\beta} + \frac{R_E}{\alpha}}$$

Make $V_{EQ} >> v_{BE}$, Insensitive to v_{BE}

$\frac{R_B}{\beta} << \frac{R_E}{\alpha}$, Insensitive to β

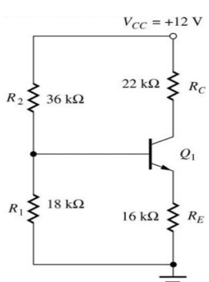
Also, choose R_1 and R_2 such that $I_1, I_2 >> I_B$

Then $I_1 \approx I_2$

The bias point (Q point) is independent of base current as well as current gain!

For design $\Rightarrow$ choose $I_1 \approx I_2 = 10 I_B$

Four-Resistor Bias Example

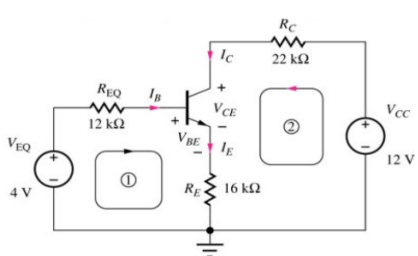


Thevenin Equivalent of Base Bias Network

$$V_{EQ} = V_{CC}\frac{R_1}{R_1 + R_2} = 4\ V$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = 12\ k\Omega$$

$$\beta_F = 75$$



$$V_{EQ} = I_B R_{EQ} + V_{BE} + I_E R_E$$

$$I_B = \frac{V_{EQ} - V_{BE}}{R_{EQ} + (\beta_F + 1) R_E}$$

$$I_B = \frac{4V - 0.7V}{12k\Omega + (76)16k\Omega} = 2.69\ \mu A$$

$$I_C = \beta_F I_B = 202\ \mu A$$

$$I_E = (\beta_F + 1) I_B = 204\ \mu A$$

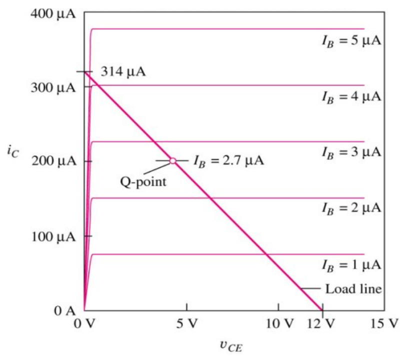
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 4.29\ V$$

Forward active region is correct

Q-point is (202 μA, 4.29 V)

Four-Resistor Bias Load-Line

- **Load-line for the circuit is:** $$V_{CE} = V_{CC} - \left(R_C + \frac{R_E}{\alpha_F}\right) I_C = 12 - 38200 I_C$$



The two points needed to plot the load line are (0, 12 V) and (314 μA, 0). The resulting load line is plotted on the common-emitter output characteristics.

I_B = 2.7 μA - the intersection of the corresponding characteristic with load line gives the Q-point: (200 μA, 4.3 V)

Four-Resistor Bias Design Guidelines

- **Choose Thévenin equivalent base voltage**

$$\frac{V_{CC}}{4} \le V_{EQ} \le \frac{V_{CC}}{2}$$

- **Select R_1 to set $I_1 = 9\ I_B$.** $$R_1 = \frac{V_{EQ}}{9 I_B}$$

- **Select R_2 to set $I_2 = 10\ I_B$.** $$R_2 = \frac{V_{CC} - V_{EQ}}{10 I_B}$$

- **R_E is determined by V_{EQ} and the desired I_C.** $$R_E \cong \frac{V_{EQ} - V_{BE}}{I_C}$$

- **R_C is determined by desired V_{CE}.** $$R_C \cong \frac{V_{CC} - V_{CE}}{I_C} - R_E$$

Four-Resistor Bias for BJT
Design Example

- Problem: Design 4-resistor bias circuit with given parameters.
- Given data: I_C = 750 μA, β_F = 100, V_{CC} = 15 V, V_{CE} = 5 V
- Assumptions: Forward-active operation region, V_{BE} = 0.7 V
- Analysis: Divide (V_{CC} - V_{CE}) equally between R_E and R_C. Thus, V_E = 5 V and V_C = 10 V; Choose nearest 5% resistor values

$$R_C = \frac{V_{CC} - V_C}{I_C} = 6.67\ k\Omega \rightarrow 6.8\ k\Omega$$

$$R_E = \frac{V_E}{I_E} = 6.60\ k\Omega \rightarrow 6.8\ k\Omega$$

$$V_B = V_E + V_{BE} = 5.7\ V$$

$$I_B = \frac{I_C}{\beta_F} = 7.5\ \mu A$$

$$I_2 = 10 I_B = 75.0\ \mu A$$

$$I_2 = 9 I_B = 67.5\ \mu A$$

$$R_1 = \frac{V_B}{9 I_B} = 84.4\ k\Omega \rightarrow 82\ k\Omega$$

$$R_2 = \frac{V_{CC} - V_B}{10 I_B} = 124\ k\Omega \rightarrow 120\ k\Omega$$